ICCAD-2017 CAD Contest in Multi-Deck Standard Cell Legalization and Benchmarks

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***Abstract*—An increasing number of multi-deck cells occupying multiple rows (e.g. multi-bit registers) are used in advanced node technologies to achieve low power and high performance. The multi-deck standard cell legalization not only should remove all overlaps between cells but also should satisfy delicate and complicated design rules with preserving the quality of the given placement by applying the minimal perturbation. In addition, the process must be fast and robust to handle the sheer number of cells in the state-of-the-art designs. For this purpose, we have defined an evaluation metric based on maximum, average cell movements, and Half Perimeter Wire Length (HPWL) as well as runtime of the legalization algorithm. In addition, we have introduced a set of benchmarks that include multi-deck cells with a range of heights (1 - 4 row heights).**

I. Introduction

The multi-deck standard cell placement legalization problem has become more challenging because of complicated design rules and design utilization at 14nm and lower technology nodes. An ideal legalization method should remove all overlaps, satisfy delicate and complicated design rules, and preserve the quality of the given placement provided by global placement or timing optimization steps. In other words, during the legalization step, *both* the average cell movement *and* maximum cell movement should be minimized. In addition, the process must be fast and robust to handle the sheer number of cells in the state-of-the-art designs. Some of the challenges in legalization of designs with advanced nodes are as follows:

- Routability gap before and after legalization: In addition to wirelength, the quality of routability is optimized during the global placement. However, in legalization the routability is degraded as the initial solution provided by global placement is perturbed. This issue has become more critical in advanced node technologies because of a high average number of pins per net (usually 4 or more), data-path modules in the netlist, accounting for special requirements associated with clock networks, accounting for timing objectives, etc.
- Physical floorplan complexity: These challenges stem from overall placement utilization, fence regions, irregular shape of the placeable area (e.g., disproportionate floorplan aspect ratios, rectilinear macro shapes, and narrow channels between large macros), boundary-pin-placement restrictions, power/ground routing resource estimation, etc.
- Complicated design rules: In addition to the constraints and rules defined to address the complexity of physical floorplan, there are other complicated design rules to address detailed routability. Some of these rules are: EDGETYPE spacing constraints among cells, and pin access and pin shorts issues [1]–[3].
- Target utilization: Most legalizers do not consider target utilization effectively. This can exacerbate situations where an input placement has local regions with high cell area utilizations. In such a scenario, it is not easy to achieve the desired timing characteristics since there may not be enough whitespace in those areas to effectively apply buffer insertion or gate sizing techniques to meet timing requirements.
- Multi-deck cells: With shrinking transistors, an increasing number of multi-deck cells occupying multiple rows(e.g. multi-bit registers) are used in advanced node technologies to achieve low power and high performance. However, it is hard to handle multi-deck cells during legalization. Legalizers should not only satisfy all the traditional constraints defined, but also the P/G alignment when placing multi-deck cells. There are some recent works trying to address Multi-deck cell legalization [4]–[7].

A. Related Work

Available legalization methods are mainly categorized as: (i) heuristic algorithms that solve the problem using a local view and (ii) formal approaches that solve the problem using a general view. Most legalization methods [3]–[5], [7]–[12] fall into the first group that resolve violations (such as cell overlaps) by exploiting a greedy search that moves cells located in violated areas to appropriate locations. Heuristic methods may lead to unnecessarily-large cell movement for designs with blockages or high utilization since they try to locally resolve violations instead of using a global approach [13].

On the other hand, formal approaches formulate the legalization problem as a mathematical model such as a network flow [13]–[15] or diffusion [16]. In flow-based methods, legalization is modeled as a minimum-cost flow problem [17] where cells (flow) are moved between source and sink nodes in order to resolve overflowed bins while minimizing cell movement.

Traditional academic legalizers have mainly addressed removing overlaps among cells on each standard row defined in the design. However, in practice there are growing challenges (including those mentioned above). Hence, new approaches are needed to overcome these challenges.

II. Design Rules and Constraints

In order to reduce the gap between academia and industry, a set of representative constraints is defined below.

A. Hard Constraints

Power/Ground (P/G) alignment of cells including single row height and multi-deck cells, row and site alignments, and fence regions [2], [12], [18] are defined as hard constraints. Each solution must satisfy these constraints; otherwise, the submission receives the maximum score.

For a design with multi-deck cells, the placement solution must satisfy P/G alignment constraints. In addition to Input/Output (I/O) pins, each cell contains two types of pins named vss and vdd that must be aligned with P/G mesh defined in the design (see Figure 1).

For cells with heights equal to odd number of a row height, this alignment is ensured by flipping cells on any rows while cells with heights equal to even number of a row height must be placed on dedicated rows. In Figure 2, this difference is illustrated. $C1$ (as a single-row height cell) in Figure 2 can be placed on any desired row by flipping because it has vdd on top and vss on the bottom. On the contrary, $C2$, which is a double row height cell, cannot be placed on $row1$ because it provides two vdd ports on the top and bottom of the cell while vss is located in the middle of the cell. Therefore, the bottom of cell $C2$ can only be placed on rows with vss grid on the bottom.

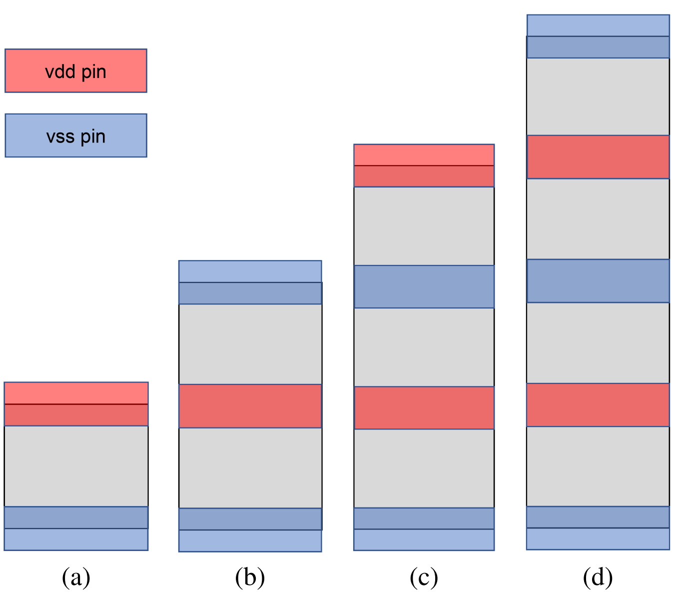

Fig. 1. Muti-deck cells with their vss and vdd pins. (a) a single row height cell; (b) a double row-height with two vss ports on top and bottom, and a vss pin in the middle; (c) a triple row height cells; and (d) a quadruple row height cell.

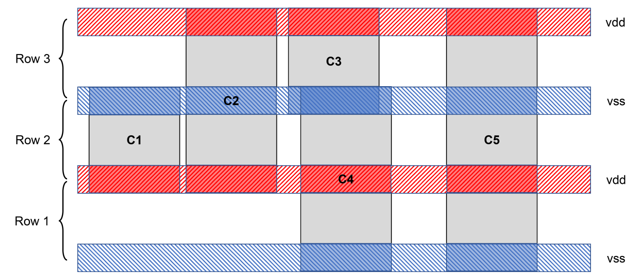

Fig. 2. An example showing multi-deck cells aligned with the P/G mesh defined in the design. $C1$ and $C3$ are single row height cells, $C2$ and $C4$ are double row height cells, and $C5$ is a triple row height cell.

B. Soft Constraints

Target utilization, maximum cell movement, and detailed routing constraints [1]–[3], [19] such as cell edge spacing, pin access and pin shorts are considered as soft constraints. If each of these constraints is not satisfied, a penalty will be enforced for the evaluation.

Comparing to designs with only single row height cells, detailed routing constraints are harder to be satisfied in designs with multi-deck cells. For example, in Figure 2, cell $C2$ should satisfy three edge spacings required between $C2$ and $C1$, between $C2$ and $C3$, and between $C2$ and $C4$.

C. Netlist Constraints

The cells in the netlist must remain the same. That is, no cell resizing, no addition/deletion of buffers, tech remapping, etc. are allowed; however, cell flipping is allowed as long as no hard constraint is violated.

III. Benchmarks

The benchmark suite for the International Conference on Computer-Aided Design (ICCAD) 2017 multi-deck cell legalization contest is provided in Library Exchange Format (LEF) and Design Exchange Format (DEF) (version 5.8) format [20]. For each design four files are provided as follows:

- **cells.lef** includes the physical characteristics of the technology library for the standard cell library, macros, and IO cells, etc.
- **tech.lef** provides the physical characteristics of the routing layers, Vertical Interconnect Accesses (VIAs), placement site types, etc.
- **design.def** includes design-specific logical and physical such as net-list connectivity, grouping information, physical constraints, cell locations and orientations, routing geometry data, P/G mesh, etc.
- **placement.constraints** is a text file including some other constraints such as maximum target utilization or the maximum displacement. Any constraint defined in this file is considered a soft constraint.

The provided benchmark suite was created from the International Symposium on Physical Design (ISPD) 2014 and 2015 placement contests ([22] and [21]) by modifying the size of cells. The global placements of all designs were generated by Eh?Placer [19]. The characteristics of the generated designs are presented in Tables I, II, and III.

IV. Evaluation Process and Scores

In order to effectively evaluate the quality of a solution, several metrics are taken into account. These metrics include the maximum cell movement (M_{max}), the average cell movement (M_{avg}), HPWL, target utilization [1], runtime time, and violations in satisfying the detailed routing constraints.

For a design z, a submitted legal placement solution $\Phi(z)$ is evaluated as follows:

$$S_{\Phi(z)} = (1 + S_t) \times (1 + S_{hpwl} + S_v) \times S_{am} \times S_{mm} \quad (1)$$

where $S_{\Phi(z)}$ denotes the total score of solution $\Phi(z)$, and S_t and S_{hpwl} are the scores computed for runtime and HPWL of the solution, respectively. S_{am}, and S_{mm} in turn indicate the scores considered for the maximum and average cell movements. Finally, S_v is the detailed routing score computed based on the number of violations in satisfying the detailed routing constraints.

A. Runtime Score

Runtime directly affects the evaluation of each team. However, there is a specified maximum runtime target. Multi-thread implementations are allowed to improve the runtime. The maximum number of threads allowed to run in parallel is 8.

The runtime score (S_t) is computed as follows:

$$S_t = \max\Big(-0.2, \min\big(0.2, 0.05\log_2(\frac{t_t}{t_m})\big)\Big) \quad (2)$$

where t_t is the runtime of the tool for generating solution $\Phi(z)$ and t_m is the median of the runtimes of all tools generating legal solutions for design z.

B. Maximum Cell Movement Score

Any cell movement is normalized by the hight of a placement row. For solution $\Phi(z)$, the maximum cell movement M_{max} is the maximum Manhattan distance of cells from their original positions divided by the height of a placement row.

The maximum movement score S_{mm} is computed as follows:

$$S_{mm} = 1 + f_{mm}(\frac{M_{max}}{100}) \quad (3)$$

Where f_{mm} is a penalty function that will affect S_{mm} if the maximum-movement soft constraint M_x defined for each design is violated. f_{mm} is defined as follows:

$$f_{mm} = \max(\frac{\sum_{c_i \in C_x} M_i}{M_x}, 1) \quad (4)$$

[1]Target utilization is defined as standard deviation from average placement utilization provided for each design.

where for solution $\Phi(z)$, C_x is a set of cells whose displacements are greater than M_x. For a given design z, if M_x is not defined, M_x will be set to the number of rows in design z.

C. Average Cell Movement Score

Average Cell Movement M_{avg} is the total Manhattan distance of movable cells divided by the number, that is normalized by the height of a placement row.

Cells in design z are grouped into K sets based on their heights. Average Cell Movement, $M_{avg,i}$, is defined as the average of the Manhattan distances traveled by the cells with heights equal to i rows. Note that the Manhattan distance is normalized by the height of the placement row. Accordingly, the S_{am} score is defined as follows:

$$S_{am} = \frac{\sum_{i=1}^{K} M_{avg,i}}{K} \quad (5)$$

D. HPWL Score

HPWL score S_{hpwl} is defined as:

$$S_{hpwl} = \max\big(\frac{hpwl_{\Phi(z)} - hpwl_{gp}}{hpwl_{gp}}, 0\big).\big(1 + \max(\beta.f_{of}, 0.2)\big) \quad (6)$$

Where $hpwl_{\Phi(z)}$ and $hpwl_{gp}$ are the HPWLs of solution $\Phi(z)$ and the initial global placement, respectively. β is a constant number. f_{of} s a penalty function to consider target utilization constraints. f_{of} is defined over square bins 88 standard-cell-row heights each, that is determined by the same method used in the ISPD 2015 contest [2].

E. Detailed Routing Score

For each design, several detailed routing constraints such as cell spacing rules and pin access issues are defined as soft constraints. Detailed routing score S_v for solution $\Phi(z)$ is computed as follows:

$$S_v = \min(\frac{N_v}{N_{cells}}, 0.2) \quad (7)$$

Where N_{cells} denotes the number of cells in design z and N_v indicate the number of violations identified by Olympus-SoC [23] for detailed routing constraints.

V. Conclusions

An increasing number of multi-deck cells occupying multiple rows (e.g. multi-bit registers) are used in advanced node technologies to achieve low power and high performance. While the single-deck standard cell legalization problem can be robustly modeled by a network flow approach [13], the multi-deck standard cell legalization is markedly harder to formulate in a robust manner. Multi-deck cells come in different types and varying heights. In this work, we have introduced a set of benchmark designs adapted from the ISPD 2014 and 2015 placement benchmarks to include multi-deck cells with

TABLE I
THE BENCHMARK SUITE CHARACTERISTICS: COLUMNS 1, 2, 3, 4, 5, 6, AND 7 SHOW THE NAME OF BENCHMARKS, THE NUMBER OF ROWS IN THE DESIGNS, THE NUMBER OF MACRO BLOCKS, THE NUMBER OF MOVABLE CELLS, THE NUMBER OF NETS, THE NUMBER OF FENCE REGIONS, AND THE NUMBER OF PRIMARY I/OS, RESPECTIVELY. THE PERCENTAGE OF SINGLE HEIGHT ROW CELLS, DOUBLE ROW HEIGHT CELLS, TRIPLE ROW HEIGHT CELLS, AND QUADRUPLE ROW HEIGHT CELLS IN THE DESIGNS ARE IN TURN PRESENTED N COLUMNS 8, 9, 10, AND 11. IN COLUMN 12, THE CELL DENSITIES OF THE DESIGNS ARE GIVEN.

Benchmark	#Rows	#Macros	#Cells	#Nets	#Fence Regions	#I/O	Cell Types %				Cell Density %
							1xH	2xH	3xH	4xH	
des_perf_b_md1	300	0	112679	122951	12	374	94.8	5.20	0.00	0.00	54.98
des_perf_b_md2	300	0	112679	122951	12	374	90.47	6.02	2.01	1.50	64.69
edit_dist_1_md1	361	0	130661	133223	0	2574	90.31	6.12	2.04	1.53	67.47
edit_dist_a_md2	400	6	127414	134051	1	2574	90.31	6.12	2.04	1.53	59.42
fft_2_md2	171	0	32281	33307	0	3010	89.62	6.56	2.18	1.64	83.12
fft_a_md2	400	6	30625	32090	0	3010	89.57	6.59	2.19	1.65	32.41
fft_a_md3	400	6	30625	32090	0	3010	93.42	2.19	2.19	2.19	31.24
pci_bridge32_a_md1	200	4	29533	34058	3	361	90.39	6.07	2.02	1.52	49.57

TABLE II
THE CHARACTERISTICS OF THE P/G MESH IN THE PROVIDED BENCHMARKS.

	P/G Layer				
	M1	M2	M3	M4	M5
Rail width (μm)	0.51	0.58	3.50	4.00	4.00
Rail spacing (μm)	1.49	20.00	14.00	20.00	14.00
Track utilization %	11	6	27	24	30

TABLE III
THE HPWLS OF THE GLOBAL PLACEMENTS, THE MAXIMUM MOVEMENT CONSTRAINT (M_x), AND THE TARGET UTILIZATION CONSTRAINT (d_{max}).

Benchmark	HPWL+e9	$M_x(rows)$	$d_{max}\%$
des_perf_b_md1	2.11	–	67
des_perf_b_md2	2.14	–	95
edit_dist_1_md1	4.01	15	100
edit_dist_a_md2	5.10	–	100
fft_2_md2	0.45	20	100
fft_a_md2	1.09	–	100
fft_a_md3	0.95	20	62
pci_bridge32_a_md1	0.45	–	80

a limited range of heights (1 - 4 row heights). While multi-deck cells come in a wider range of heights, we believe this benchmark suite helps illustrate the essence of this problem. The ultimate measures of a legal placement's quality are satisfaction of utilization and design rule constraints, detailed routability and minimal perturbation to the timing quality of the input global placement. As a proxy for the minimal perturbation to an input placement, we have defined a metric based on maximum, average cell movements, and HPWL as well as runtime of the legalization algorithm. Our goal is to motivate researchers to solve this problem. We will report the results from contestant teams in the upcoming ICCAD 2017.

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