

1. 先進入 ProblemE_test 資料夾
>cd ProblemE_test
2. 開啟 cadence encounter
>encounter (請參照 CIC 的路徑)
3. 執行 run_case1.tcl
encounter 1 > source run_case1.tcl
4. 檢驗 report 中是否有出現 violation
5. exit 結束

=====
run_case1.tcl 內容. 若有需要, 請依照指令調整檔案位置

```
set init_verilog "./data/case1.v"  
set init_top_cell top  
set init_design_netlisttype Verilog  
set init_lef_file {./data/tech.lef ./data/blocks.lef}  
set init_gnd_net {VSS}  
set init_pwr_net {VDD1 VDD2 VDD3}  
set defHierChar /  
init_design  
defIn ./data/case1_output.def  
verifyGeometry  
verifyConnectivity -noAntenna
```

=====
驗證 Geometry 結果

```
*** Starting Verify Geometry (MEM: 555.9) ***  
  
VERIFY GEOMETRY ..... Starting Verification  
VERIFY GEOMETRY ..... Initializing  
VERIFY GEOMETRY ..... Deleting Existing Violations  
VERIFY GEOMETRY ..... Creating Sub-Areas  
..... bin size: 12000  
VERIFY GEOMETRY ..... SubArea : 1 of 1  
VERIFY GEOMETRY ..... Cells : 0 Viols.  
VERIFY GEOMETRY ..... SameNet : 0 Viols.  
VERIFY GEOMETRY ..... Wiring : 0 Viols.  
VERIFY GEOMETRY ..... Antenna : 0 Viols.  
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.  
VG: elapsed time: 0.00  
Begin Summary ...  
Cells : 0  
SameNet : 0  
Wiring : 0  
Antenna : 0  
Short : 0  
Overlap : 0  
End Summary  
  
Verification Complete : 0 Viols. 0 Wrngs.  
  
*****End: VERIFY GEOMETRY*****  
*** verify geometry (CPU: 0:00:00.0 MEM: 61.9M)
```

=====

驗證 Connectivity 結果

VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Tue Apr 18 16:36:26 2017

Design Name: top
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (3000.0000, 3000.0000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary

End Time: Tue Apr 18 16:36:26 2017
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0 MEM: 0.000M)

=====

GUI 畫面顯示沒有錯誤產生

- GUI 操作指令 “f” 為畫面置中, “z”為放大, “Z”為縮小, 移動畫面請用鍵盤上的上下左右鍵

